An Introduction to Prognostic Fingerprint Technology©

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Abstract

Avionic systems demonstrate at least 40% 'no fault found' rates and for the civil sector, the estimated cost was $100,000 per aircraft per annum in 1997. The same factors that induce this waste cost mobile phone manufacturers $4.5 billion per annum.

Neural-network test equipment and advanced processing techniques can generate successive 'Fingerprints' to monitor the condition of avionic systems over time.

Voltage signals on significant points in a system are measured using high impedance probes. The voltages are processed and recorded as **vectors** which can be arranged in logical order to create an electronic map (or **fingerprint**). The Map comprises three important subsystems that have to be developed and connected to create the complete fingerprinting system.

The construction of the fingerprint is a predefined software procedure that captures, analyses and exploits the data in multi-layered arrays. Recognising what type of processing is relevant enables the software to characterise the circuit and build a unique fingerprint. To reduce time and processing power, a minimal set of vectors must be defined for each task. Duplication in any test point selection process risks missing critical data.

Keywords: Avionics, no fault found, neural network, health management, intermittent fault, artificial intelligence, data acquisition, vector map

Introduction

Avionic systems in military and commercial aircraft demonstrate at least 40% 'no fault found' rates (NFF) and it was estimated that for the civil airline industry alone, the cost impact was $100,000 per aircraft per annum in 1997. The same factors that induce this waste cost mobile phone manufacturers $4.5 billion per annum.

A fusion of the sensory capabilities of analogue intermittent fault finding systems having detection levels in the nano-seconds with advanced processing and data exploitation techniques offers the potential to monitor the condition and degradation over time of an individual electronic item or system. This would be achieved by generating a 'Fingerprint' of the test subject at certain points in time.

The Technology

As part of the inexorable pursuit of improved safety, performance, availability, efficiency and affordability of technology, it is crucial to validate the integrity and reliability of electrical and electronic products and their major components and sub-components. This requirement is equally valid across civil and Defence aviation, space, renewable energy, transport and

telecommunications. Health Management and Prognostics (HMaP) is a common strategy in the aerospace sector, particularly for structural integrity and the integrity of mechanical systems, but it is far less common for electrical and electronic systems. PFT™ (Prognostic Fingerpring Technology) is a HMaP solution that is rapid, repeatable and effective, and applies to civilian and military aircraft along with other sectors.

The assurance of components has never been more pivotal as operating budgets are reduced and as electronics are increasingly used as the foundation from which to challenge the boundaries of science, technology and understanding. There is a clear need to develop and refine a unique and revolutionary new HMaP approach to increasing the integrity and reliability of electrical and electronic equipment.

HMaP solutions aim to improve the sustainment and predictability of equipment reliability, with some HMaP methods being applicable to electrical/electronic equipment. Indeed, there are digital mapping techniques that can map a circuit but these techniques are limited, with most of them being extremely time-consuming and necessitate dismantling to basic component parts. While none of these methods should be individually discredited, they could be enhanced tremendously with the primary aim of improving the detection of intermittent faults, which are the major root cause of NFF issues.

Analogue neural-network systems can monitor multiple circuits simultaneously and continuously with no digital sampling, no digital averaging effects and no single-point-in-time constraints. The result is an ability to detect the smallest effective change in ohmic characteristics, of well below 50 nanoseconds duration[1]. This capability could be exploited to extend the concept into more technologies, to reduce the time to rectify faults and to embed the intellectual knowledge in the equipment rather than train and qualify expert technicians.

By connecting intermittent fault finding equipment, for example an aircraft Line Replaceable Unit (LRU), it is possible to capture an electronic 'fingerprint' of the unit-under-test's operation. This would include baseline ohmic values, radio frequency-induced impedance tests, relay contact impedance and resistance and ground capacitive effects. To fully exploit these capabilities, specific algorithms would be developed that could weight and filter the results appropriately and which would take into account changes in operating modes and environmental conditions. The fingerprint history could be stored on an RFID (Radio Frequency Identification Device); the RFID could then be interrogated and compared directly with the current fingerprint, with the resulting analysis confirming to what extent the item's electronic integrity had been maintained and/or identifying emergent trends where the component was starting to deteriorate and, thus, trend towards failure.

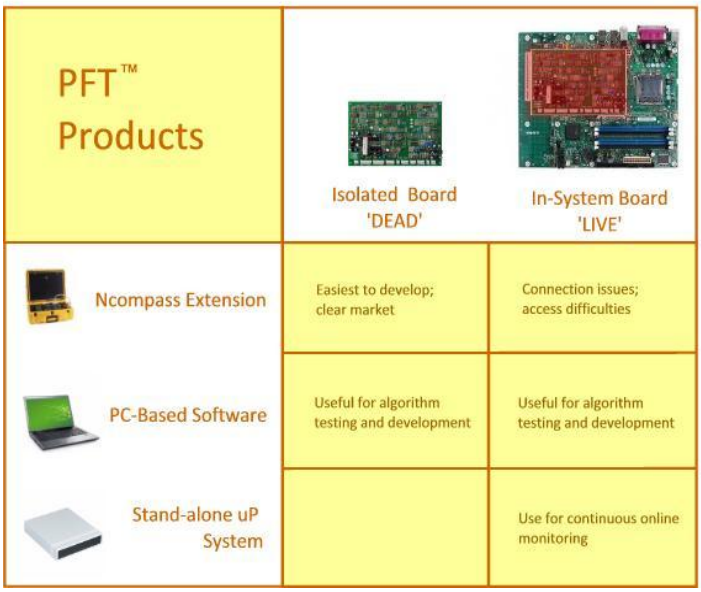


***Figure 2** The PFT™ core concept can be implemented in a number of ways, depending on the host system used to run the fingerprinting algorithm and the state of the board to which it is applied. The grid shows separate products that could be developed.*

In principle the PFT™ system would be

[1] Recently verified by a 3rd party at 8 nanoseconds duration.

able to generate the fingerprint of any electronic circuit. The procedure used to create the fingerprint can be applied equally effectively to printed circuit boards that, perhaps because of a suspected fault have been separated from the unit in which they operate, and also boards that need to be tested *in situ* whilst powered. Although the same fingerprinting process can apply in each case, there is a practical distinction between a 'live' and a 'dead' board (Fig. 2). With a failed board, the multiple line intermittent fault finding test equipment provides a convenient way of reading various characteristics[2] from a large number of test points on a complex circuit. Where the test lines have to be excited in some way to elicit a response, test pins can be driven with low voltages under the control of the intermittent fault finding technology.

In contrast, a live board does not have to be powered externally to facilitate data collection. Gaining access to points on the board may be complex where LRUs have not been designed with sufficient test points and with access to those points during normal operation. However, built-in data capture could be designed into the circuit-board or for some cost-effective applications, retrospectively added to provide the necessary data capture. This data would be a raw data stream and it could be either captured and stored, and then downloaded or transmitted to the PFT^{TM} server. Clearly another solution could be an intrusive scheduled data capture by taking the test equipment physically to the site of the faulty system; however, this provides only diagnostic capability as opposed to enhanced prognostic capability.

The PFT^{TM} system can be packaged in a variety of ways (Fig. 2). The product can be a simple extension to existing intermittent fault finding equipment or it could be a PC-based application designed to analyze raw data files captured in a number of ways. The device could range from a stand-alone instrument with low speed processing acting on a much restricted set of circuit test points to embedded complex circuit sensing and wireless transmission to Cloud data storage for remote interrogation. The advanced diagnostic and indeed prognostic capability becomes effective when a fleet-size number of devices of the same type continuously send data to a central server via the web. The variety and quantity of sources result in the accumulation of raw data to an extent that permits detailed characterization of that particular board/circuit design. In this way continuous condition monitoring is possible at low cost. The more devices that are monitored, the better the overall knowledge of the system and the lower the unit monitor cost becomes. Emanating from the original design compromises, repeated faults occur and it is this knowledge that directs technicians to achieve reduced repair times. By combining an expert system with data collection, storage and analysis, the fault history of the design can be made available to the PFT ^{TM} system; taken one step further, and the deviation from the normal - or 'Gold' - fingerprint could be identified and thus the failure period of Prognostic Fingerprinted interval determined.

The third issue of importance is the resolution of the fingerprint. The underlying fingerprint will reflect circuit connects and component properties; however, and this is particularly true for live systems, there will be a superimposed fuzzy layer originating from the many different ways the circuit behaves during normal operation or under excitation. Therefore, the challenge will be to see a clear fingerprint through the fog, and use the emerging picture to identify faults and/or developing faults in the device under observation. A high resolution fingerprint will reflect the tolerances of the components used on a specific printed circuit board (and component variation) and will differ very slightly across boards of the same type. It will also change over time as components age; a trend that will be important to understand and trace. Therefore, this high resolution may not actually be desirable - a lower resolution generic fingerprint that will apply to all instances of that circuit may be more preferable. The final resolution will allow problems to be diagnosed on a faulty board returned from field

[2] Characteristics could range from simple ohmic, capacitance or impedance values or devised testing regimes specifically compiled for PFT^{TM}.

operation, or provide confidence that the board has a level of integrity; of course the latter of these outcomes would mean that the intermittent fault is somewhere else in the system. Moreover, there may be even an ability to diagnose both outcomes on a legacy board that had never previously been characterized as individual serial numbered items could be compared to fingerprints held on the server for that particular model.

Just detecting a change in the fingerprint is not the ideal solution. It would far more useful if the diagnostic system was able to associate this alteration with a specific component or to a particular region of the board by correlating this with the actual fault and by linking this to the original symptom experienced. A mere change in the fingerprint only affords us the baseline knowledge that the circuit is deviating from the norm and therefore might be leading up to some kind of failure or, worst case, has already failed.

Any PFT ™ system development will explore these concepts, though an extension of intermittent fault finding equipment capabilities applied to dead boards and this would be the preferred first step towards developing a universal PFT ™.

The fingerprinting technology will complement 'no fault found' diagnostic systems based on analogue neural-networks that have been shown to be effective in dealing with nanosecond duration spikes. There may be some overlap in capability when live systems are fingerprinted: the after-effects of brief failure events may cause a detectable disturbance which propagates through the circuitry.

The technological challenges of a PFT™ system will be explored so that the level of difficulty and effort required to develop a prototype system can be gauged.

A PFT ™ System Concept

The principle of a PFT™ system is illustrated in Fig. 3. Voltage signals are picked off significant points on the board[3] using high impedance probes so as not to interfere with normal circuit operation in the case of live boards. The voltages are processed in a variety of ways to generate indicators that correlate in some way with circuit operation. The set of indicators for a complete measurement event are referred to as a **vector**. The vectors corresponding to different modes of operation can be arranged in logical order to create an electronic map (or **fingerprint**) that spans **function space**. For a dead system, this may just be a matrix of voltages corresponding to connection and excitation sequences.

Figure Three details three important subsystems that have to be developed and connected to create the complete fingerprinting system. Data acquisition for the most part is straightforward and can be performed effectively by existing intermittent fault finding equipment. The construction of the fingerprint is a software procedure that uses existing artificial intelligence methods. However a critical element in building an effective system is the processing layer, and recognising what type of processing is relevant and meaningful. Only if appropriate **information** is extracted or distilled from the huge quantity of values collected from the data acquisition layer will the analysis software be able to characterise the circuit and build a unique fingerprint. An even greater challenge is to extract a minimal set of vectors that will span operation space – it is likely that many of the signals from the data acquisition layer

[3] Sometimes it is necessary to use any points that are accessible, but for complex circuitry it is common for the manufacturer to make important test points available as a header on the edge of the board.

encode the same information, and a lot of processing effort is then spent for no useful return. However, it may not be possible to avoid duplication in any realistic test point selection process. Missing important data is more critical than having to deal with data repetition. The penalty for repetition is slower processing time.

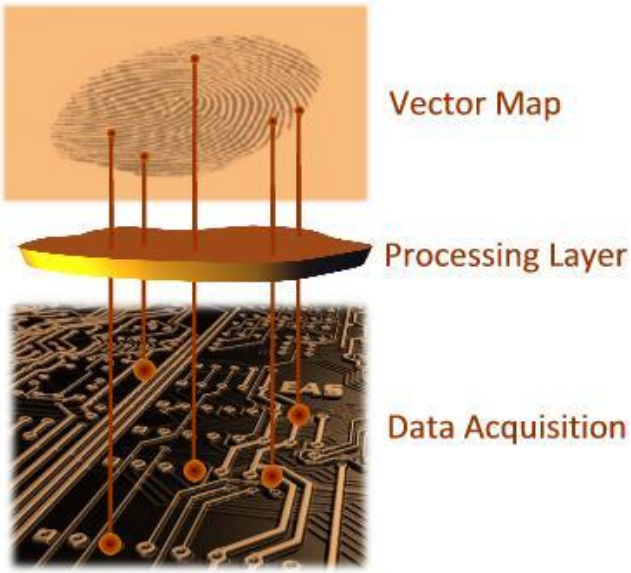


Figure 3 *The basic fingerprinting process*

Interpreting Voltages on Unpowered Board

An unpowered board can be tested for continuity between all the available test points. For N test pins, this will mean 2 x (N-1) parallel measurements giving N(N-1) results[4]. This is an efficient process and will immediately reveal continuity problems. The risk arises with boards populated with non-linear active circuits such as logic gates. Many CMOS logic gates have separate clamping diodes inserted on the input paths as shown in Fig. 4.

The diodes perform a useful protection function during normal operation, but if the devices are unpowered when a positive external voltage is applied to the pad, then the test voltage will find a path to the power rail via the top protection diode and try to power up the whole circuit. A voltage level of greater than 0.7V is generally needed to initiate this effect. If microprocessor devices are inadvertently activated, the effect on line voltages throughout the circuit is complex and unpredictable. Repeatability between tests is the key to constructing a fingerprint and random code execution and the rapid switching of floating devices make repeatability impossible, and so research into these effects is vital to develop a suitable solution to overcome them.

At CMOS switch gates with no specific input protection (such as analogue switches) gates are particularly vulnerable to applied test voltages. Diode bridges like those in Fig. 4 also form within the structure of the complementary CMOS switch. These diodes are not robust and are easily destroyed (Fig. 5). A current flow of only 20 mA can be sufficient to cause irreversible damage. Even with smaller currents, DC offsets and crosstalk result. The high gain of parasitic transistors can cause SCRs to form ultimately resulting in device latch-up. Using the existing neural network intermittent fault finding equipment as a data collection device, the voltage and current flow can be limited below acceptable levels and also benefit from the synaptic arrangements provided .

It is possible to test unpowered digital circuitry, but great care is needed to avoid damaging associated circuitry and thought must be given to interpreting the results. Probing with very small voltages will most likely give repeatable results, but there is a need to guard against diodes masking much of the digital circuitry and restricting the information that finds its way into the fingerprint.

[4] A factor 2 is included because the continuity should be tested in both directions to take into account diode links.

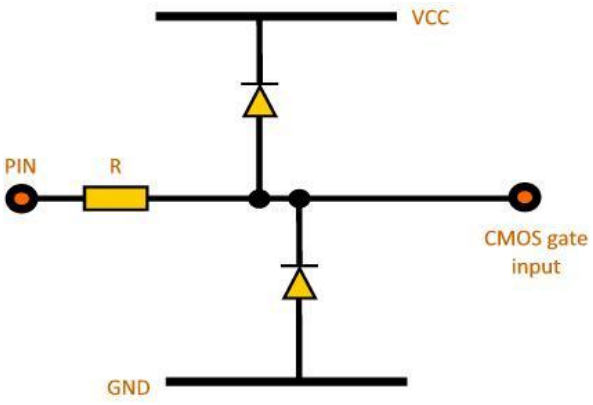


Figure 4 *CMOS logic gates include overvoltage clamp diodes as shown.*

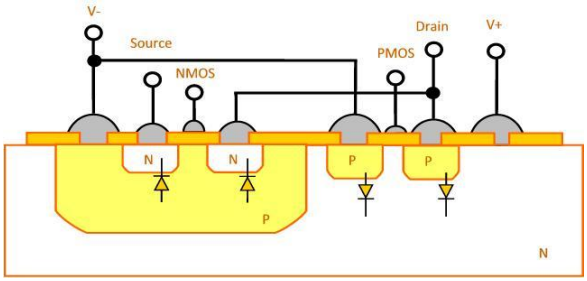


Figure 5 *At die level diodes exist when the device is unpowered.*

Powered Circuits: Digital Blocks

Live circuits can be easier to analyse. Any system under test can be divided into digital and analogue blocks. Digital systems will exhibit switching transients of the type shown in Fig. 6. These transient do not usually affect system operation because the true line status only needs to be established and stable after a recognised set up time. Synchronisation is under the control of a system master clock. For example, if memory needs to be read, the binary address is presented on the address bus, the device enabled and read lines are activated and in response the contents of the memory are transferred to the data bus. After a short delay to allow the voltages to stabilise, the data is read by the processor. This methodology is quite resilient, particularly as the voltage band corresponding to logic zero can range from -0.1 V to + 1.2 V, and logic one can be any value above +2.2 V.

The voltages (logic levels) on lines, once stable, are of little interest and will rarely tell us any more on the physical condition of the board and components than what is revealed by the transients. The actual logic levels on the lines are a function of execution state of the stored program, and whilst the device may exhibit errors associated with incorrect program operation, these are generally not the concern of a fingerprinting system. Problems of this type can often be traced by a systematic approach to testing because they are repeatable and predictable. Locating the problem can be difficult and a conventional logic analyser or a JTAG boundary scan debugger[5] makes the task easier. Automatic test pattern generation devices are also used with a variety of scan options to assist with diagnosis.

Standard digital test equipment will not deal with unpredictable intermittent faults. In some applications these cannot be ignored because the potential consequences of a single random pulse system failure are so serious. In this situation high speed analogue equipment is used.

A fingerprinting system will not attempt to replicate the operation of these conventional test devices. Nor will the system try to correlate and interpret logic levels on signal buses. Instead the focus should be on transients and noise, both of which deal with low-level circuit and component operation, and in particular grounding issues (including high ground path impedance, ground loops and inadequate separations of digital and analogue grounds). CMOS-based digital systems only consume power during logic state transitions and because

[5] This is an inbuilt self-test feature within complex devices that can be accessed via special pins on the chip that can accept and deliver serial information and is the current state-of-the-art [8], [9]

all switching is synchronised to master clocks, this can give rise to high-current short-duration pulses that can spread through the whole system as electromagnetic radiation. This is particularly a problem with long, high impedance lines that have a tendency to act as very effective antennae. Floating inputs are particularly troublesome as noise pick up can rapidly switch logic gates exacerbating noise problems. Capacitive coupling also offers another path for noise to invade signal lines. Noise levels are a particularly good indication of the health of the circuit and should feed into the PFT [TM] system. The noise spectrum gives clues to the noise source: the characteristic frequency may be related to components which are clocked at that frequency. But noise issues frequently arise from poor design or layout resulting in undesirable linkages between different circuit blocks, and it is possible that a fingerprinting system may be a useful way of directing design improvements in existing systems.

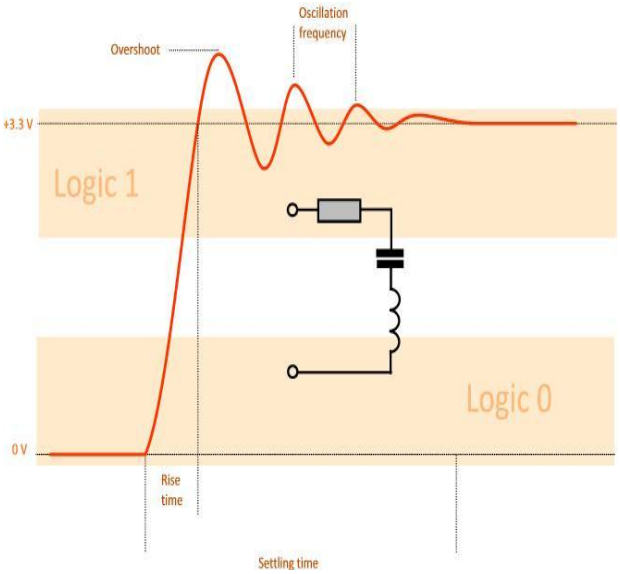


Figure 6 *A digital line switching from logic level 0 to 1 might act as shown. If the system is underdamped as a result of high capacitance, the rise time can be very high with no overshoot. The ideal is the critically-damped response that minimises overshoot and settling time [10].*

For digital circuits therefore, voltage levels should ideally be processed to derive the following:

1. Noise amplitudes and frequencies
2. The step response rise time
3. The step response overshoot
4. The step response settling time
5. The step response oscillation frequency

Frequency spectra can be constructed via the FFT procedure (Fast Fourier Transform) but an FFT is a time consuming procedure that may involve 10^6 calculations. It is important to restrict the number of transformations according to the time available for analysis. The analysis may also reveal unwanted resonances. There may also be an advantage in buffering the data so that instances of narrow spikes are captured in raw form and not lost whilst the processing is taking place.

Powered Circuits: Analogue Blocks

Analogue circuitry block testing requires different techniques to those used with digital blocks. In the analogue case, the correlation between the voltages at different points on the circuit is the most effect way of obtaining fingerprinting information. Whilst transients are of interest, the effect of voltage amplifiers with their complex feedback makes it difficult to relate the shape of the transient to a meaningful result. Voltage averaging over a suitable time period is often effective for analogue testing. Fig. 7 represents a non-inverting amplifier and the relationship between TP2 and TP1 is a function of the resistor values and the static properties of the operational amplifier. The dynamic properties of the

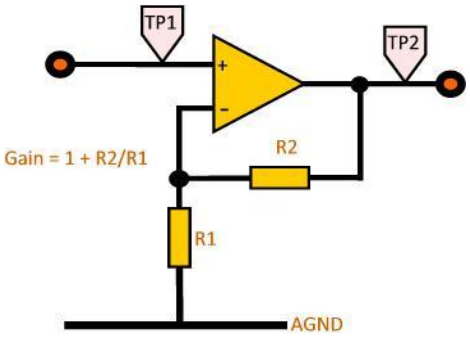


Figure 7 *The action of the operational amplifier and the two resistors can be derived from the voltages on test points 1 and 2*

device can be found from the phase difference between input and output as a function of frequency (effectively a Bode plot). And noise is particularly important because of inevitable amplification by circuit elements.

Intermittent connections can cause temporary instability and this can be trapped by an PFT^{TM} system

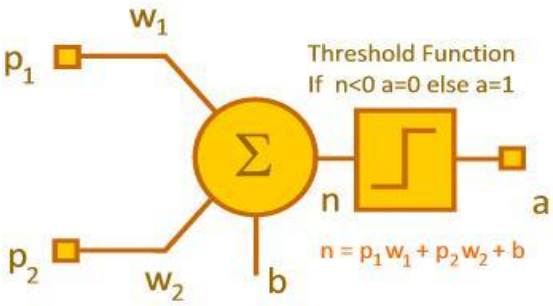
The fingerprinting process is seen to complement conventional methods and could result in better diagnosis capabilities both through isolated fault identification and continuous in-line monitoring to warn of developing problems.

Artificial Intelligence

Artificial Intelligence (AI) is the name for a collection of data analysis techniques that deal with the automatic processing of huge volumes of raw data to reveal hidden patterns which would otherwise appear to be random. AI is distinguished from conventional statistical methods by the use of learning algorithms. There are a vast number of procedures in common use which target different classes of data management task. These procedures include expert systems, fuzzy logic, constraint programming and artificial neural-networks. The challenge is to find the most appropriate technique, and although all the procedures are notionally 'intelligent' the true intelligence originates in the selection of the correct procedure by the human developer. The developer also has to provide the tool with some guidance on what the key indicators could be.

Artificial neural-network (ANN) applications are applicable where a pattern (or order) is buried in a mass of data and are candidates for the prognostic fingerprint technology. An ANN is an attempt to replicate the operation of a neuron in the human brain. A software model of the artificial neuron provides a flexible approach where design and configuration changes are easily made. Hardware neurons are only required with high speed data streams when a sub-microsecond response is essential.

Fig.8 illustrates the basic operation of an artificial neuron. The circle with the summation symbol represents the body of the neuron. The values of the weights w_1, w_2 and the bias, b, are essentially the 'knowledge' or memory content of the neuron.



TEST POINT	p1	p2	Expected	Actual	Error
1	75	21.5	1		
2	31	2.3	0		
3	64	20.2	1		
4	93	35.9	1		
5	4	3.2	0		
6	23	5.9	0		
7	79	25.7	1		
8	63	24.9	1		
9	98	26.4	1		
10	44	16.2	1		
11	20	1	0		
12	27	0.1	0		
13	54	19.2	1		
14	94	37.2	1		
15	74	28.2	1		
16	17	-3.9	0		
17	41	6.3	0		
18	29	6.7	0		
19	3	-8.1	0		
20	73	18.9	1		
21	62	24.6	1		
22	98	29.4	1		
23	29	7.7	0		
24	83	14.9	1		
25	0	8	0		
26	80	17	1		
27	36	11.8	0		
28	5	-6.5	0		
29	36	3.8	0		
30	7	-5.9	0		

Figure 8 *The most basic of artificial neurons is shown above. There diagram shows two inputs p_1 and p_2, weights w_1 and w_2 and the bias b. The neuron is trained by feeding the set of 30 data points shown in the grid.*

Data is presented on the inputs and are modified by the weight on that input line. Finally the adjusted data is added together with the bias. Based on the final value (n, in Fig. 8) the neuron 'fires' (output = 1) or it does not (output = 0). The neuron output can then be connected to the inputs of other neurons to form a complex network.

All neurons are initialised with random weights and bias. Fig. 8 shows a table of training data. The objective is to teach the neuron to give the expected output for each of the test points by modifying the weights and bias through an iterative training process. The first point in the table has values $p_1 = 75$ and $p_2 = 21.5$. These are fed to the artificial neuron. The output is calculated by multiplying each input by the weight then applying the threshold function. If the output matches the expected value, nothing happens. If it does not, the weights and bias are adjusted slightly to make the neuron more likely to give the expected output next time around (the training rule). The 30 test vectors are presented over and over again, cycling perhaps as many as 10,000 times, until the errors are minimised. Once the system has 'learnt' about the data, it can be applied to new data where the expectation is unknown and used to predict the output. In this single-neuron configuration, a basic curve-fitting procedure is applied to the data set, but by extending the number of lines into the neuron and adding more neurons in multiple layers, the capacity to learn and classify increases dramatically to the extent that underlying patterns can be found in very complex data.

Feed-forward networks of this type are trained by a procedure called supervised learning – a data set with known outputs is required for the training stage. The training process is called back-propagation.

In many applications we do not know what to expect when data is presented to the network and therefore supervised learning is inappropriate. However, there are other ANN configurations that can learn without being shown what to do[6]. The complex Hopfield network in Fig. 9 is based on this principle and is typically used for pattern recognition. As an example, a network of 256 neurons connected after this fashion is used to read handwriting. The procedure would be to use a scanner to create a 16 x 16 binary pattern of each letter that is representative of the character shape. In the training phase, the system is presented with all the letters of the alphabet until each character is associated with one of the neurons (meaning the neuron weights will take on the binary value corresponding to that character). In the operational phase, handwritten characters, perhaps quite different from the formal character shapes, are presented to the trained network by imposing the scanned pattern on the neurons. The neurons are then fired at random (overwriting the imposed values) until the network locks on the nearest stable or stored value. This is then the letter the system considers the handwritten symbol to be.

A network like this performs some of the tasks required of the PFT ™. However the Hopfield network may not have the capability to deal with the huge amount of raw data inevitably associated with the fingerprinting of complex electronic circuits.

A better configuration for the fingerprinting application is the Self-Organising Feature Map (SOFM). This type of network has the complexity to deal with a single **state vector** which encodes all the information taken from the raw voltage activity over the entire circuit at a particular point in time. This vector is fed to a network of typically 1024 neurons. The neurons are initially assigned random vectors of the same dimension as the state vectors. As

[6] Think of the way a child learns to recognise faces or walk – no one needs to tell the child how to move muscles or what the parts of the face are.

the state vector is presented to the network, those neurons that are closest[7] are drawn towards the state vector and altered by a proportional amount[8]. In this way, the neurons cluster around the known state vectors. The vector values can be presented as a colour-coded 2-d grid which is, in effect, the system fingerprint (Fig. 10).

The fingerprint forming the SOFM, could well be dimensional. A different testing algorithm could produce each dimension so that there are layers of SOFM; this could be either frequency based or just a different test regime.

Further investigation could develop a suitable neural network that will enable a fingerprint to be built. Such investigation must consider other options such as evolutionary networks, genetic algorithms, temporal difference learning and associative learning.

While the performance of a neural network-based solution cannot be 100%, it does provide a level of confidence of fingerprint recognition. Therefore, a move to the high confidence at 70-80%, provides a step-change in filter-bench capability that could be adopted globally, and consequential savings for the electronics and electric industries.

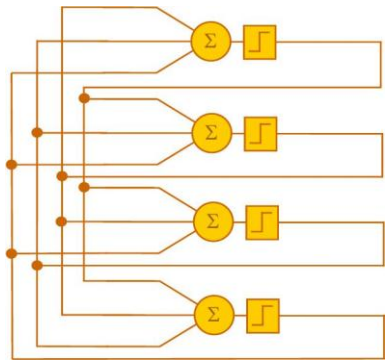


Figure 9 *Simple neurons are connected with feedback to form a Hopfield network*

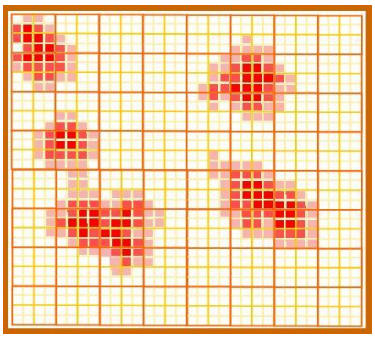


Figure 10 *This SOFM map has 1024 neurons (32 x 32) and the clustering suggests 4/5 distinct modes of operation for the system. In the test phase following training, a test vector finding the closest neuron to be away from the clusters could be the indication of a fault condition (or merely the system being used in a new way that did not occur during training).*

Current Research

Circuit fault finding is time-consuming and costly whilst considerable research work has already been conducted on the application of neural networks to PCB and circuit fault diagnosis, and the state of current knowledge should be the start point for the development of the PFT®.

From academic and industry publications there is little evidence of success at building fingerprinting systems, and there is certainly no product close to market. A lot of work has been done on the basics: sources of error; modelling systems; manipulating data; uses of neural networks. Building on some solid results combined with the advantage of having access to a stream of high quality data through emerging intermittent fault finding systems would suggest the objective of developing a prototype prognostic fingerprinting technology in 3 years is feasible.

Zio [12] reviews the entire topic of reliability engineering, including the role of artificial neural networks. Qi *et al* [13] reviews the no-fault found (NFF) condition and stress how important and prevalent the problem is. They give clear guidelines on how the effect should be assessed. They conclude with a warning:

[7] The 'closeness' is determined by taking the scalar product of the vector components.
[8] This is rather like the way footballers on a field react to the ball – the closer they are to the ball the more they are drawn to it.

'It is a good business and engineering practice to start with the premise that field returns are field failures, unless some alternative reason can be verified. It must not be assumed that a returned product that passes tests is necessarily free from faults. Companies should start with the premise that field returns are field failures. NFF statistics should not be used to ignore, mitigate or transfer the field return problem to a non-failure status.'

Söderholm [14] looks at more specifically ways to deal with the NFF phenomenon. Sorensen [15] has considered how traditional test equipment misses nanosecond glitches that are often associated with the NFF condition. He advocates a hardware neural network and makes a case for its use. As specified earlier, the proposed prognostic fingerprinting system introduced here will complement systems of this type and this technology has been highly successfully in detecting and isolating intermittent faults. The patented analogue neural network is in fact the Ncompass® 4000 which has taken over 16 years to develop and is produced by Universal Synaptics Corporation [16]. This analogue neural network is also used by Total Quality Systems to continuously monitor hundreds of circuit paths to detect intermittent faults down to 8 ns duration [17]. Refer to Cauwenberghs' paper [18] for an example of an analogue neural network implementation using analogue VLSI parts. Hardware implementations of neural networks in general are reviewed by various authors [19, 20, 21].

There are two standard ways of implementing an electronic fault diagnostic system: a model based system or a data-led approach. Cunningham [22] describes a model-based system for fault diagnosis in power supplies and claims a better than 80% fault location performance. Isermann [23] gives a full description of model-based detection. De Kleer and Williams [24] warn of the possibilities of differences between the artefact and the model and the effect on diagnosis, particularly troublesome in the case of multiple faults.

Neural networks show benefits over single path or switching conventional techniques in the case of multiple simultaneous faults. This is a relatively common condition because an external causative agent (such as a voltage spike) is likely to be non-specific and affect more than one component. It is also possible the board design may suffer from poor fault partitioning (one fault can lead to conditions that can quickly induce another)[9]. There are many techniques that can identify faults, but it is rather more difficult to pinpoint that fault to a component or an area of the board. If this cannot be done, the fault repair capability is limited.

Stošović and Litovski [25] make similar observations:

'The recent growth of mixed analogue and digital circuits complicates the testing problem even further. It becomes more complicated to determine a set of input test signals and output measurements that will provide a high degree of fault coverage. There is also a timing problem of testing the circuits even on the fastest automated equipment.'

In an instructive book chapter, they go on to explain why neural networks are applicable to this problem. Spense [44] has described how much more difficult fault finding is becoming with progressive component and PCB miniaturisation. Defining a test strategy is extremely time-consuming and not guaranteed to be effective, or worse, give ambiguous results that demand extensive investigation.

Litovski *et al* [27] tested simple analogue circuits using a feed-forward network. A training set was generated for a specific circuit by anticipating the output for a variety of inputs (using information from the data sheets) and recording data in the time and frequency domains to

[9] It is important to be aware of problems that can be induced by PCB design, particularly if an autorouter is used [11].

compare with functioning circuits. The trained network was then applied to circuits with induced faults. A 'simulate before test' approach was also proposed by Manikandan and Devarajan [28] and tested with rudimentary circuits. Sutton [29] attempted to map each circuit component that can fault to a specific neuron. The disadvantage is that a fault condition must first be triggered in order that the network may be trained to store the fault condition. Fanni *et al* [30] looked at a neural network for the analysis of analogue circuits and focussed on the influence of feature extraction techniques such as Fourier Transforms, Wavelets and Principal Component Analysis on the effectiveness of the system.

Mismar and AbuBaker [31] apply a feed-forward neural network to the analysis of transient behaviour and cite the most significant articles in this field ([32] – [38]). Litovski and Andrejević [39] give a very simplistic example of feed-forward network applied to a CMOS amplifier. Returning to basic principles, Milovanovic and Litovski [40] describe the fault conditions associated with CMOS circuitry. Czaja and Kowalewski [41] also stimulate an analogue circuit with a step voltage and analyse the response, making a comparison against what is expected (another example of simulate before test). Yuan *et al* [42] use kurtosis (a measure of the tail property of a statistical distribution) to feed a neural network that is designed to identify faults in analogue circuits.
There are other ways to build up a board fingerprint. The most obvious is thermal imaging (Vichare and Pecht [43]) which maps the Joule heating associated with current flow over the board. However there are two significant problems: The resolution tends to be very low because conduction, convection and radiation blunts sharp boundaries, and the response time for thermal processes is of the order of 10 s, very far from the 100 ns resolution needed to detect fast transient events. However thermal imaging would certainly show the degradation of components and perhaps bad solder joints and could be used as another dimension of the fingerprinting outlined (Tragner, [26]).

Spense [44] scanned the magnetic field over the surface of the board and extract the underlying pattern using an ANN. Though promising, the idea was not developed further.

It is also possible to test boards using optical inspection techniques and X-ray imaging.

A novel approach in the aviation industry is patented ARCSAFE® system that uses a "low energy high voltage" method to induce a "wire safe" arc event at the defect site, providing non-destructive identification of an insulation defect. The system can provide fault identification across a small air gap between conductors, typical of wires, which have temporarily shorted together as a result of chafing or mechanical breakdown of the insulation, and then cause problems during flight. However, this testing has to be limited to simple circuits such as cable harnesses, because the high voltage would damage electronic components and may well be restricted on certain aircraft configurations and systems. Overall while it seems a proven solution, its limitations and the limited market exposure, it is not seen a competitor to PFT™ [45].

Benefits

The benefits of a fully developed PFT ™ system are:

1. *Safety Improvement.*

a. By continually monitoring a Line Replaceable Unit (LRU) and mapping the shift in its fingerprint, engineers can increase the availability of the asset within reasonable cost. With advanced algorithms as an outcome of this R&D, it may be possible to predict failures of assets through using PFT ^{TM} life monitoring.
b. Engineers can make a knowledge-based rather than an assumption-based decision leading to better fault finding decisions therefore optimising fixing the fault correctly the first time.
c. Effective prevention of NFF problems using PFT ^{TM} has second order benefits with respect to Flight Safety:

    i. Provides a "knowledge-based" approach to intermittent fault correction removing the guess-work type impost on pilots and maintenance staff.
    ii. NFFs cause aborted sorties which aircrew have to re-plan and re-execute. As well, the morale sapping uncertainty from the impact of re-work in having to instigate additional repair activity to fix repetitive intermittent problems is difficult to quantify.
    iii. The loss of system functionality due to intermittent faults can erode mission effectiveness, the level of performance or the level of redundancy of the system.

2. *Availability Improvement.*

a. Serviceability is a 'point in time' attribute whereas Availability[10] is more about the ability for an asset to perform across its life. The ability to ascertain the integrity of an asset quickly at any stage of an asset's life is an important factor in ensuring an asset performs with the minimum of unscheduled maintenance.
b. Understanding and manage the fleet of assets across multi-platforms by fingerprinting each asset, logging its signature on RFIDs and providing a central database will provide enhanced availability for assets whilst reducing the cost of ownership of those assets.

3. *Cost Reduction*

a. Fixing faults correctly the first time will be assisted by the PFT^{TM} regime coupled with intermittent fault detection and isolation.
b. Reduced platform downtime increases availability and increases profit margins on Availability-based centric contracts (ie 'Power by the Hour' contracts).
c. Increases MTBFs by keeping assets fitted to their parent platform for longer and reducing the need for unscheduled maintenance activities.
d. Enables knowledge-based sentencing of unnecessary returns or warranty issues.
e. Drives a new maintenance regime that drives out the practice of speculative component changes.
f. Reduces the supply chain for the asset and its associated components.
g. Reduces the need for expensive ATE to be deployed with operators, and instead introduces pan-platform usage.
h. Increases the reputation of the OEM/MRO for meeting mission effectiveness, on time and within budget.

[10] The UK MOD's Reliability & Maintainability policy documents define 'Availability' as "the ability of a system to be in a state to perform as required, under given conditions, at a given instant, or over a given time interval".

Conclusions

With Avionic systems demonstrating increasing "no fault found" failure rates now exceeding 40%, the most advanced neural networks and artificial intelligence can be applied to reduce the time to make systems serviceable and reduce maintenance costs. Discrete test equipment is available to find intermittent faults and this capability can be extended by the application of artificial intelligence. Proven fully serviceable system characteristics can be mapped and then continually compared to the performance of system elements down to component level. This Prognostic Fingerprint Technology© (PFT^{TM}) traps voltage and current vectors using techniques applicable to the technology under test, stores the data and outputs the analysis to the technician. The result is failed or failing component identification which then can be removed from service before catastrophic failure.

Recommendations

A target application be selected which has a high probability of success and that funding be sourced to develop a functional PFT^{TM} as a lead product. The technology can be subsequently expanded to encompass all of the uses of this technology across infrastructure and transport.

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